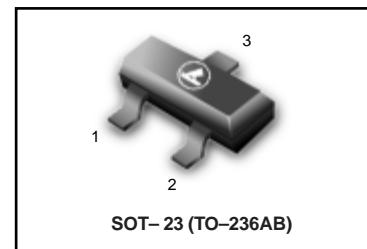


30V P-Channel Enhancement-Mode MOSFET

● APPLICATIONS

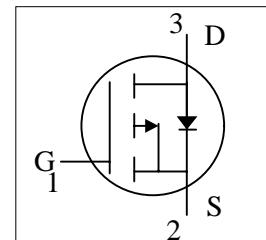
- 1) Advanced trench process technology
- 2) High Density Cell Design For Ultra Low On-Resistance
- 3) We declare that the material of product are Halogen Free and compliance with RoHS requirements.

LP2305LT1G



● FEATURES

- 1) $V_{DS} = -30V$
- 2) $R_{DS(ON)}, V_{GS} @ -10V, I_{DS} @ -4.2A = 70m\Omega$
- 3) $R_{DS(ON)}, V_{GS} @ -4.5V, I_{DS} @ -4.0A = 85 m\Omega$
- 4) $R_{DS(ON)}, V_{GS} @ -2.5V, I_{DS} @ -1.0A = 130m\Omega$



● DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2305LT1G	P05	3000/Tape&Reel
LP2305LT3G	P05	10000/Tape&Reel

● MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-to-Source Voltage	V_{DSS}	-30	V
Gate-to-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	-4.2	A
Pulsed Drain Current(Note1)	I_{DM}	-30	A
Total Power Dissipation	P_D	1.4	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Thermal Resistance-Junction to Ambient(Note2)	$R_{\theta JA}$	140	°C/W

1. Repetitive Rating: Pulse width limited by the Maximum junction temperature

2. 1-in² 2oz Cu PCB board

LP2305LT1G
●ELECTRICAL CHARACTERISTICS (Ta= 25°C)
STATIC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	V(BR)DSS	-30	—	—	V	VGS = 0 V, ID = -250 μA
Gate Threshold Voltage	VGS(TH)	-0.7	—	-1.3	V	VGS = VDS, ID = -250 μA
Zero Gate Voltage Drain Current	IDSS	—	—	-1	μA	VDS=-24V, VGS=0V
Gate-to-Source Leakage Current	IGSS	—	—	±100	nA	VDS = 0 V, VGS = ±12 V
Drain-to-Source On Resistance(Note3)	RDS(on)	—	53	70	mΩ	VGS = -10V, ID = -4.2 A
		—	64	85	mΩ	VGS = -4.5 V, ID = -4 A
		—	86	130	mΩ	VGS = -2.5 V, ID = -1 A
Forward Diode Voltage	VSD	—	—	-1	V	VGS = 0 V, ISD = -1A
Forward Transconductance	gFS	7	11	—	S	VDS = -5.0 V, ID = -5 A

DYNAMIC

Input Capacitance	Ciss	—	826.18	—	pF	VGS = 0 V, f = 1.0 MHz, VDS= -15 V
Output Capacitance	Coss	—	90.74	—		
Reverse Transfer Capacitance	Crss	—	53.18	—		
Total Gate Charge	QG	—	6.36	—	nC	VGS =-15 V,VDS = -4.5V ID = -4A
Gate-to-Source Gate Charge	QGS	—	1.79	—		
Gate-to-Drain Charge	QGD	—	1.42	—		
Turn-On Delay Time	td(on)	—	11.36	—		
Rise Time	tr	—	2.32	—		
Turn-Off Delay Time	td(off)	—	34.88	—	ns	VDD = -15V, RL =3.6 Ω ID = -1A, VGEN = -10V RG = 6 Ω
Fall Time	tf	—	3.52	—		

3. Pulse Test: Pulse width≤300μs, duty cycle ≤2%.

LP2305LT1G

ELECTRICAL CHARACTERISTIC CURVES

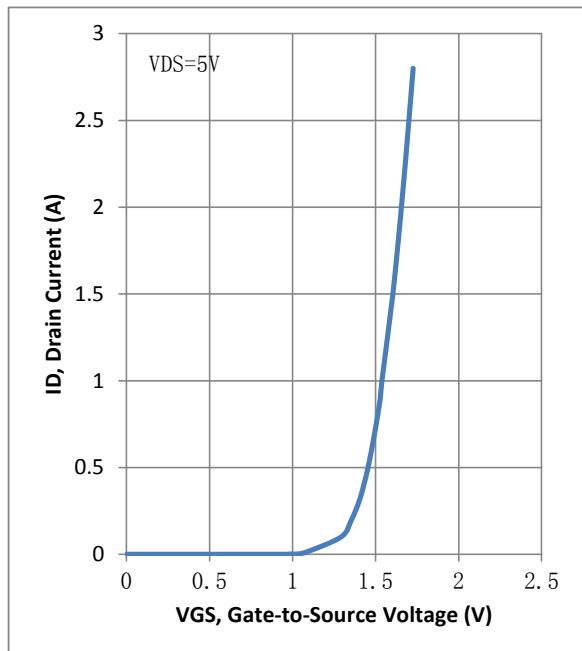


FIG. 1 Transfer Characteristics

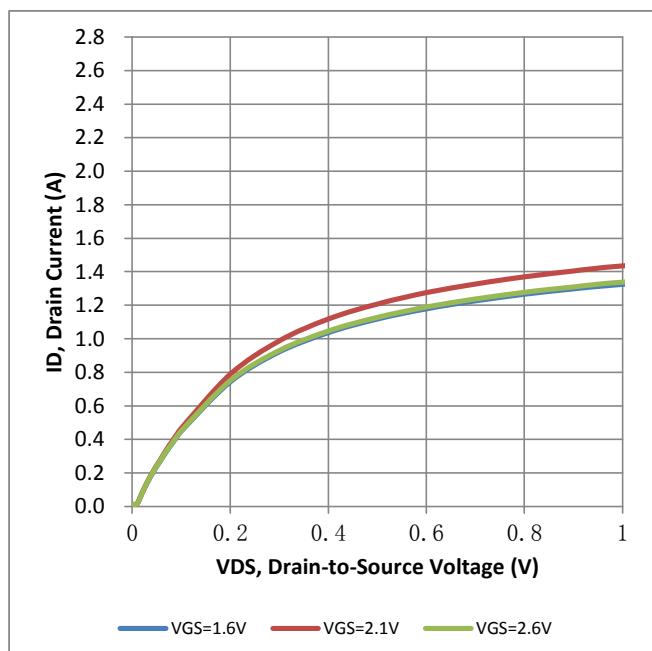


FIG. 2 On-Region Characteristics

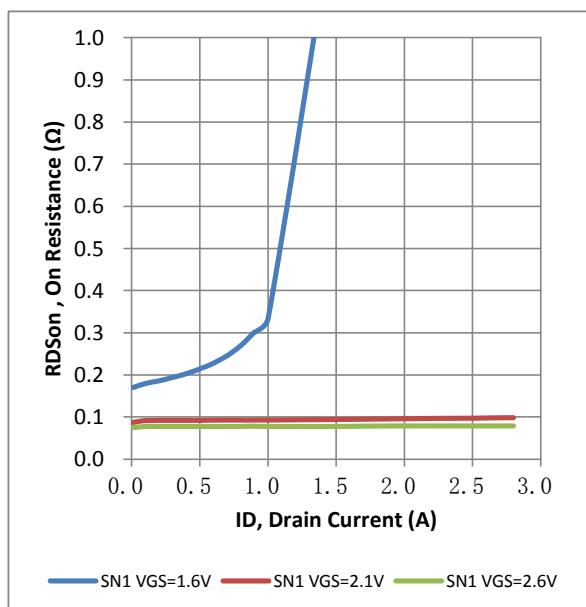
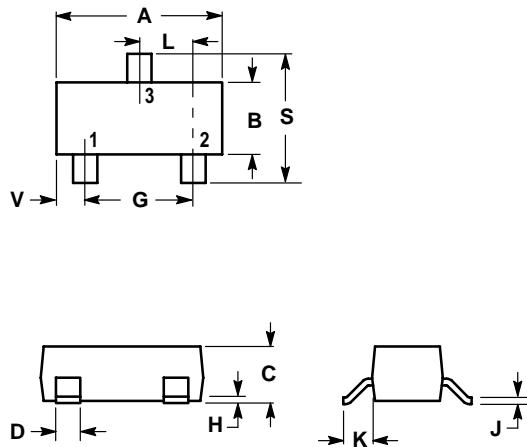


FIG. 3 On-Resistance Versus Drain Current

LP2305LT1G
SOT-23
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

